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1. A system to manage energy usage of a processor, comprising:

a data communication network;

a transmitter, coupled to the data communication network, to invoke a protocol state machine to send a packet, to wait for an acknowledgment of receipt, and to prepare for a periodic transmission of additional packets;

a receiver, in communication with the transmitter coupled to the data communication network, to receive, process, and verify the packet and send an acknowledgment of receipt;

a buffer, coupled to the protocol state machine, to store the packet; and

a timer, in communication with the transmitter and the receiver, to cause a periodic pattern of packet transmission and reception, wherein the processor is adapted for use in an energy conscious device.

2. The system of claim 1, wherein the data communication network includes at least one of the Internet and an Intranet.

3. The system of claim 1, wherein the transmitter begins in a high power, high clock rate mode.

4. The system of claim 1, wherein the transmitter performs tasks to create packets for transmission.

5. The system of claim 4, wherein the tasks include at least one of dividing data into packets, adding protocol headers, and computing checksums.

6. The system of claim 1, wherein the transmitter enters a low power, low clock rate mode while waiting for an acknowledgment from the receiver.

7. The system of claim 6, wherein the transmitter awakens as at least one of a timer sounds and an incoming packet buffer reaches a low water mark.

8. The system of claim 1, wherein the receiver begins in a low power, low clock rate mode.

9. The system of claim 1, wherein the receiver enters a high power, high clock rate mode when the buffer reaches capacity or a high water mark.

10. The system of claim 1, wherein a frequency setting and a power level of the processor are determined by the transmitted or received packet.

11. The system of claim 10, wherein the periodic pattern in packet transmission and reception are used to manage the frequency setting and power level of the processor.

12. (Amended) An article comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following:

sending a data packet over a data communication network to a receiver protocol state machine that stores the data packet in an application buffer;

waiting for an acknowledgment of receipt of the data packet from the receiver protocol state machine; and

arranging for a transmission of additional data packets.

13. (Amended) The article of claim 12, wherein instructions are provided to a transmitter protocol state machine to send the data packet while in a high power, high clock rate mode.

14. (Amended) The article of claim 13, wherein instructions are provided to the transmitter protocol state machine to enter an idle low power, low clock rate mode upon completion of data packet transmission.

15. (Amended) The article of claim 14, wherein instructions are provided to the transmitter protocol state machine to return to a high power, high clock rate mode upon a sounding of a timer.

16. (Amended) The article of claim 12, wherein an application buffer and a timer cause periodic patterns in data packet transmission, which are used to manage power and frequency of a processor.

17. (Amended) An article comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following:

receiving a data packet from a transmitter protocol state machine over a data communication network;

depositing the data packet in an application buffer;

processing and verifying the data packet; and

transmitting an acknowledgment of receipt of the data packet to the transmitter protocol state machine, wherein the transmitter protocol state machine prepares for transmission of additional data packets.

18. (Amended) The article of claim 17, wherein instructions are provided to a receiver protocol state machine to obtain delivery of the data packet, to store the data packet in

the application buffer, to process the data packet, and to send the acknowledgment of receipt of the data packet.

19. (Amended) The article of claim 18, wherein instructions are provided to the receiver protocol state machine to enter an idle low power, low clock rate mode upon obtaining delivery of the data packet.

20. (Amended) The article of claim 19, wherein instructions are provided to the receiver protocol state machine to enter a high power, high clock rate mode when the application buffer reaches a maximum capacity.

21. (Amended) The article of claim 17, wherein the application buffer and a timer cause periodic patterns in data packet reception, which are used to manage power and frequency of a processor.

22. (Amended) The article of claim 17, wherein the data communication network includes at least one of the Internet and an Intranet.

23. A method of managing energy usage of a processor using a plurality of transmitter protocol state machines and a plurality of receiver protocol state machines in a multiple layer architecture within a data communication network, comprising:

relaying, from the plurality of transmitter protocol state machines, a data packet to a receiver protocol state machine;

receiving the data packet;

storing the data packet in at least one application buffer;

switching a processor clock mode and a power mode;

processing the buffered data packet;

transmitting the processed data packet; and

delivering the processed data packet to the data communication network.

24. The method of claim 23, wherein the plurality of transmitter protocol state machines commence at an appropriate clock rate for one application among a plurality of applications.

25. The method of claim 24, wherein each application fills one application buffer in a plurality of application buffers.

26. The method of claim 25, wherein the plurality of applications are blocked when at least one application buffer reaches capacity and all buffers contain sufficient data.

27. The method of claim 26, wherein the plurality of receiver protocol state machines are invoked to process the data in the buffers.

28. The method of claim 27, wherein the plurality of transmitter protocol state machines switch the processor clock mode and the power mode to an appropriate mode to process data.

29. The method of claim 23, wherein the plurality of transmitter protocol state machines begin in a high power, high clock rate mode, and the plurality of receiver protocol state machines begin a low power, low clock rate mode.

30. The method of claim 23, wherein the data communication network is at least one of the Internet and an Intranet.